CHW 261: Logic Design

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Prof. Hala Helmy Mohamed Zayed

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Current Administrative Position: Dean ,More

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Publications [Titles(22) :: Papers(0) :: Abstracts(21) **]**

Inlinks(0) :: Courses Files(2) | Total points :45

News

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Research Interests

Computer vision, pattern recognition, image processing and neural networks

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You are in:Home

Dr. Ahmed Shalaby

Academic Position: Lecturer

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Scientific Name:

Publications [Titles(4) :: Papers(2) :: Abstracts(4) **]**

Inlinks(6) :: Courses Files(4) | Total points :49

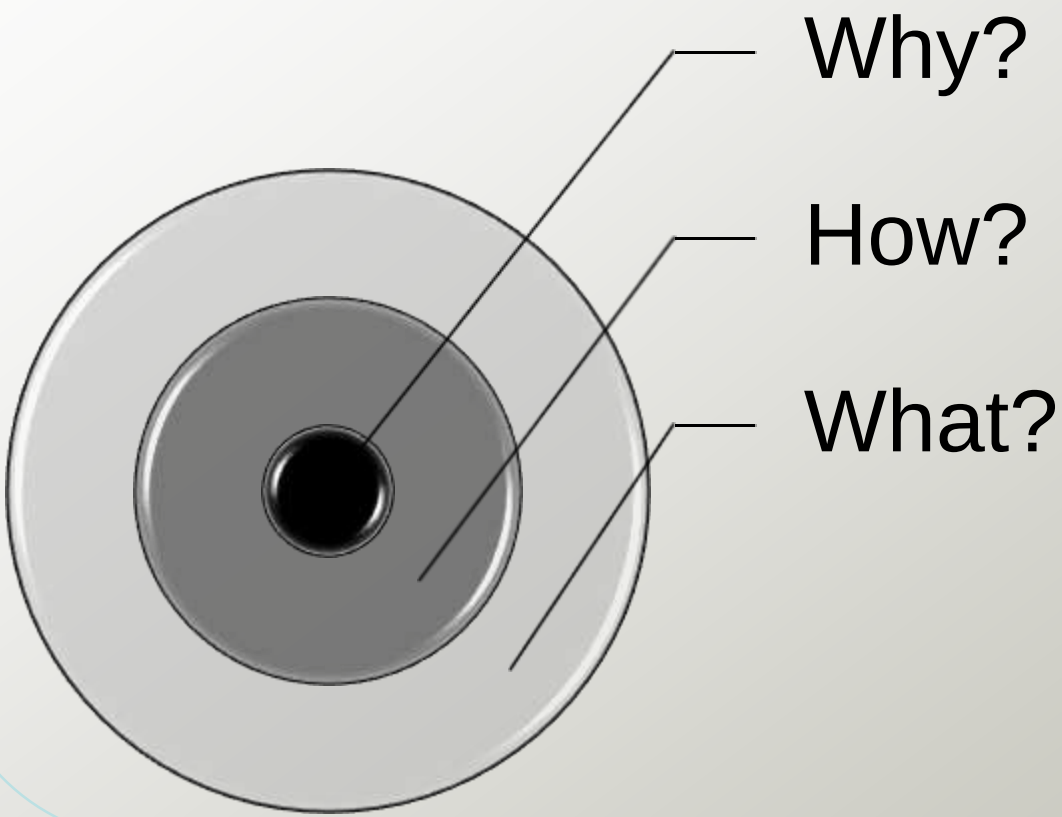
News

IOT Project Update [2016-11-14]
Smart Water Management Irrigation System (SWMIS) project moves to field test phase on November 2016. more

Research Interests

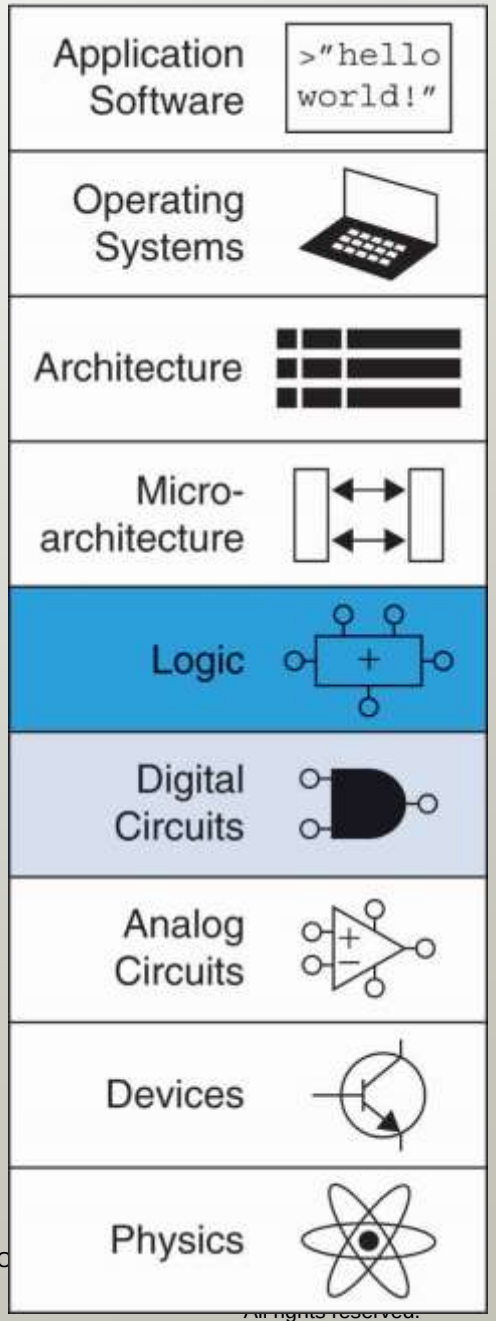
System on Chip, Network on Chip, VLSI, Embedded System, High Efficiency Video Coding (HEVC)

Study: CHW 261: Logic Design

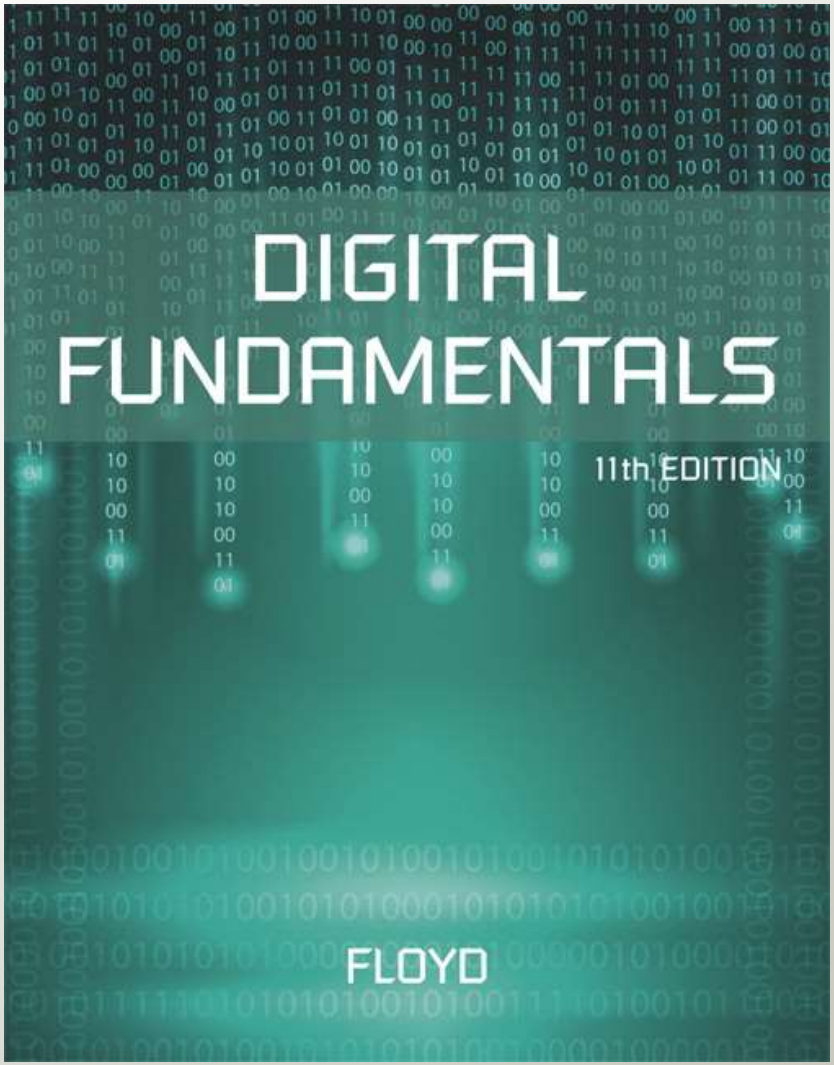


What ? Logic Design

- **Logic Design** defines the fundamentals of Digital systems, such as computers and cell phones.



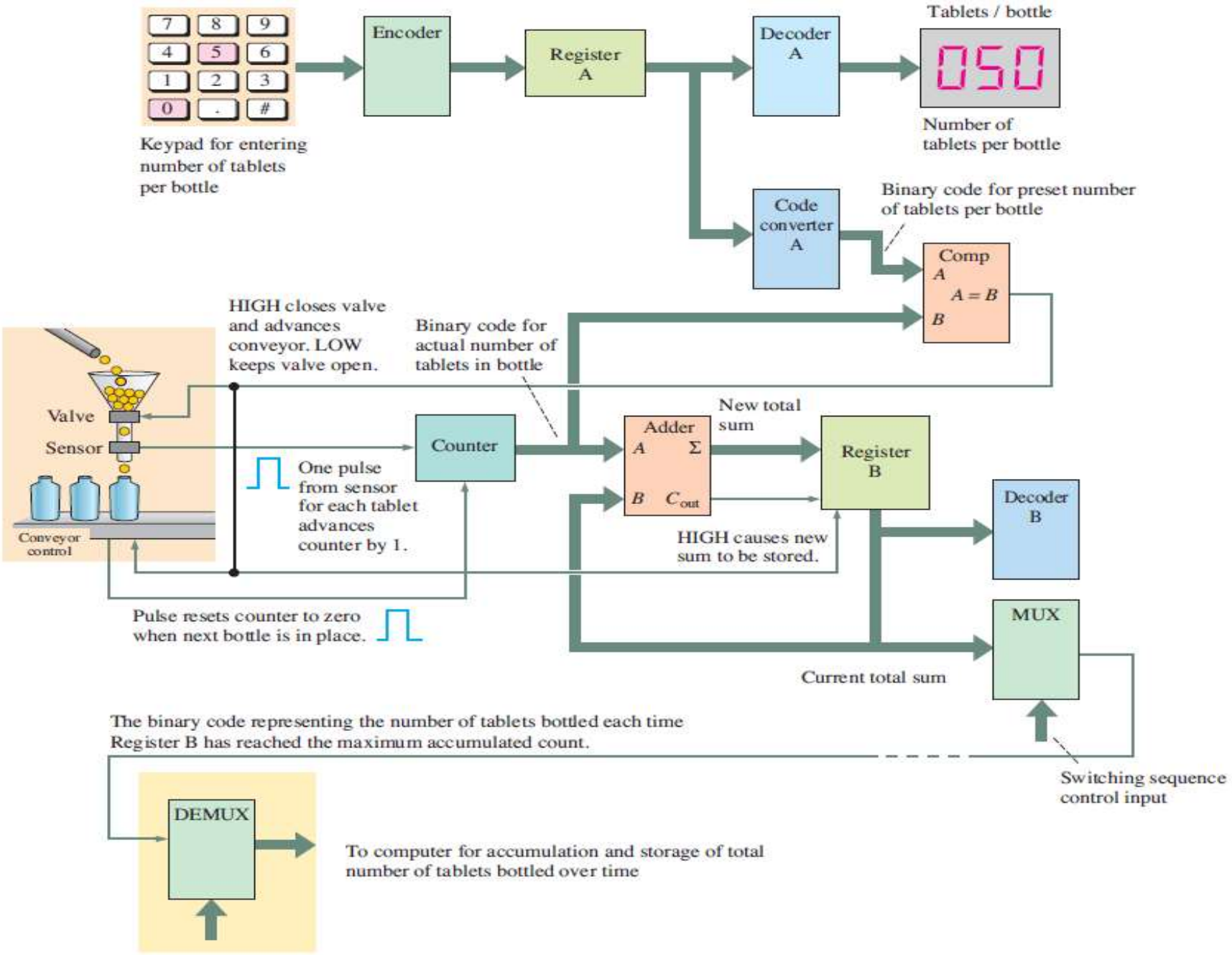
How ? Course Book



How ? Course Content

Subject
Chapter 1: Introduction Concepts
Chapter 2: Number Systems, Operations, and Codes
Chapter 3: Logic Gates
Chapter 4 : Boolean Algebra and Logic Simplification
Chapter 5: Combinational Logic Analysis
Chapter 6: Functions of Combinational Logic
Midterm Exam
Chapter 7: Latches, Flip-Flops, and Timers
Chapter 8: Shift Registers
Chapter 9: Counters
Chapter 10: Programmable Logic

Why ? Logic Design


7 8 9
4 5 6
1 2 3
0 . #
Keypad for entering number of tablets per bottle
Encoder
Register A
Decoder A
Tablets / bottle
050
Number of tablets per bottle
Code converter A
Binary code for preset number of tablets per bottle
Comp
A
A = B
B
HIGH closes valve and advances conveyor. LOW keeps valve open.
Binary code for actual number of tablets in bottle
Valve
Sensor
Conveyor control
Counter
One pulse from sensor for each tablet advances counter by 1.
Adder
A Σ
B Cout
New total sum
Register B
HIGH causes new sum to be stored.
Decoder B
Pulse resets counter to zero when next bottle is in place.
MUX
Current total sum
The binary code representing the number of tablets bottled each time Register B has reached the maximum accumulated count.
Switching sequence control input
DEMUX
To computer for accumulation and storage of total number of tablets bottled over time

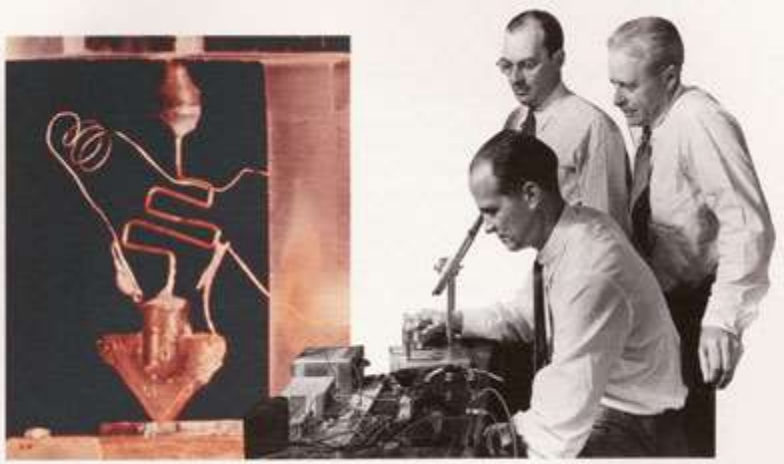
Assessment

Final-Term Examination	65
Mid-Term Examination	10
Practical Examination	15
Oral Examination	10

Projects:

- Digital Clock.
- Traffic Light.

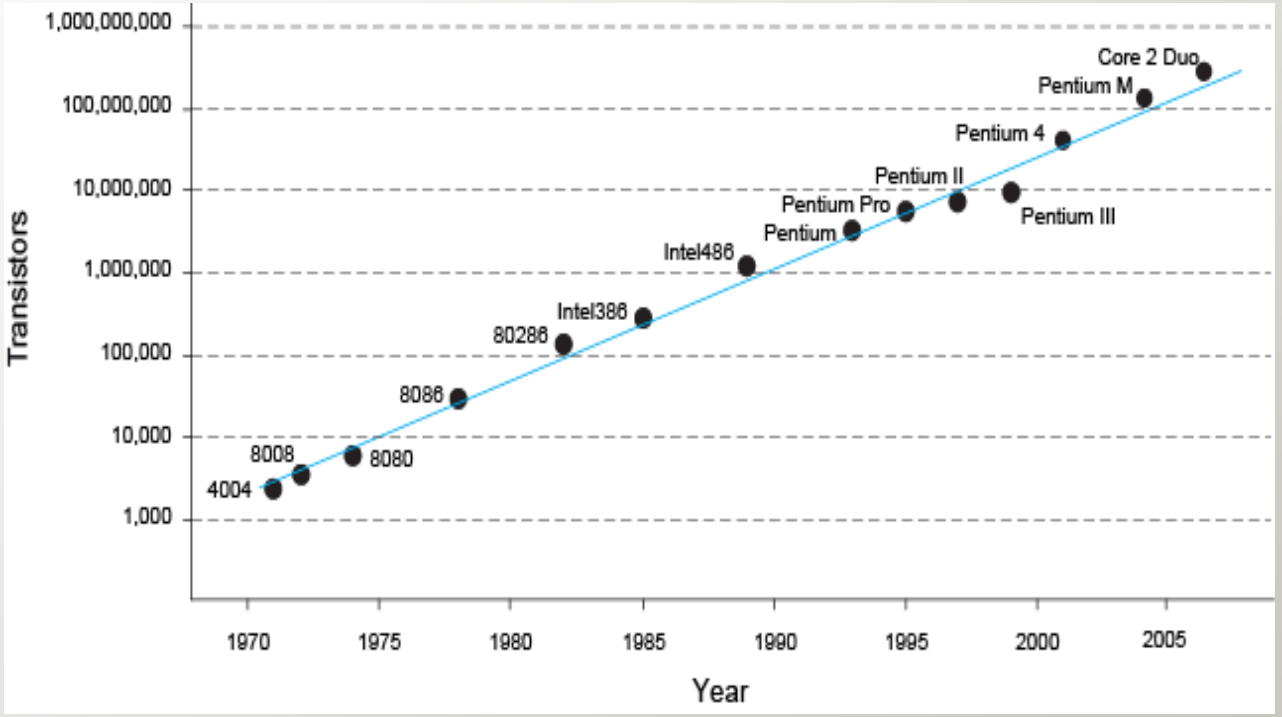
History Snapshots



- **1947:** The **transistor** was invented
- **1958: Integrated Circuit (IC),** A transistor was integrated with resistors and capacitors on a single semiconductor chips.
- **1971: first commercially microprocessor**, Intel Corporation produced the Intel 4004 , giving birth to a family of **processors on a chip**.
- **1981:** The IBM PC (5150) was announced.

Moore's Law

- **Moore predicted that number of transistors on a chip doubles every 1.5 years.**



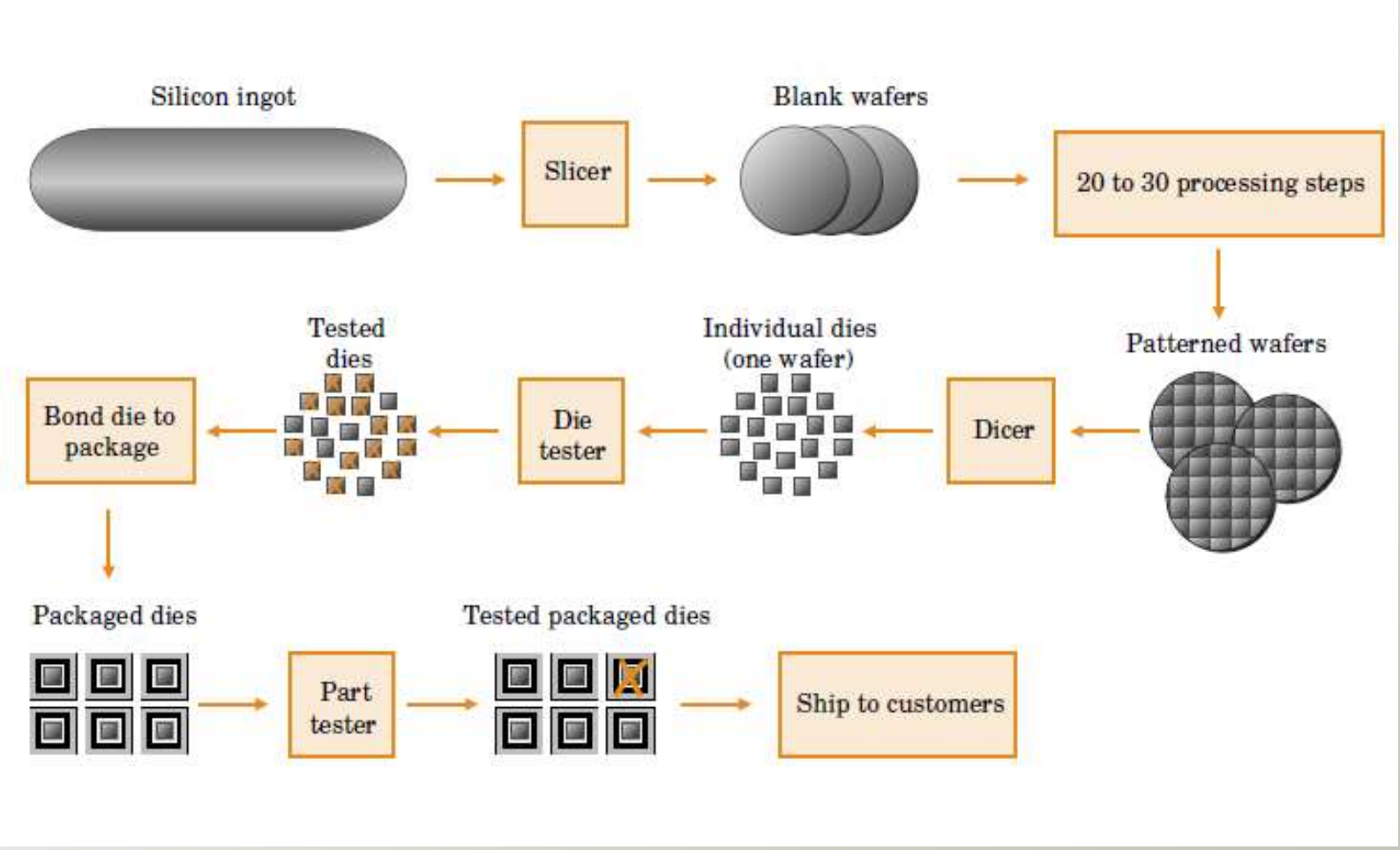
Moore's Law

- **Moore predicted that number of transistors on a chip doubles every 1.5 years.**
- Moore's Law implies :
  - Processor speed doubles every 1.5 years.
  - Memory density doubles every 1.5 years.
  - Size of chip design team doubles every 1.5 years.
  - Chip cost remains the same.

Digital System (How)

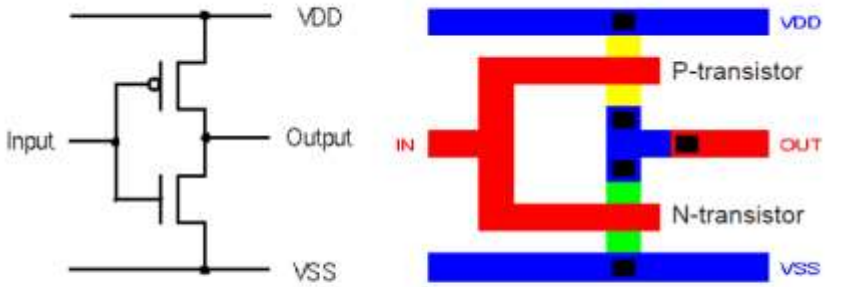
Silicon Run 1 2nd Edition.rm

Digital System (How)



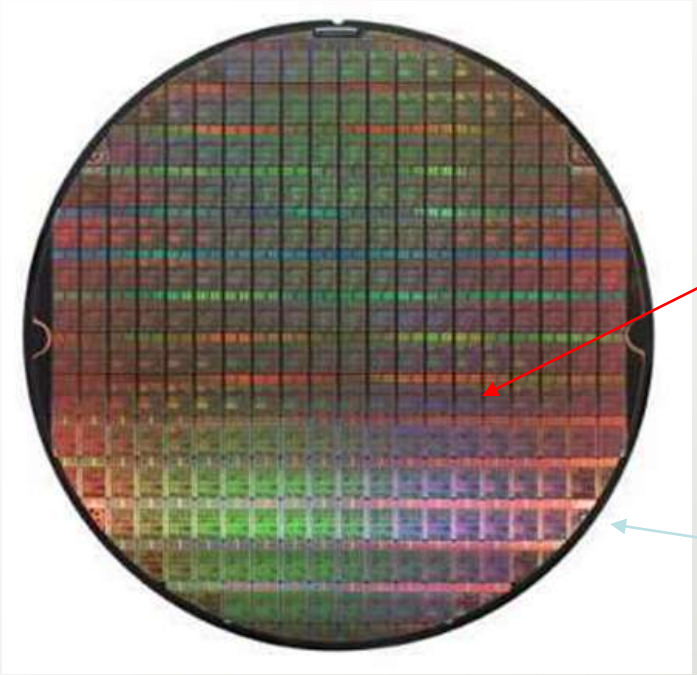
IC Manufacturing Process

- Transistors and wirings are made from many layers (10−15) built on top of one another **(Mask Layers)**.
- Each successive mask layer has a pattern that is defined using a mask similar to a glass photographic slide.
- The first layers define the transistors.
- The last layers define the metal wires between the transistors (Interconnects).
- **Metal layers** are named metal 1 (m1, usually for GND/VDD), metal 2 (m2, usually for input and outputs), etc.



The CMOS Inverter

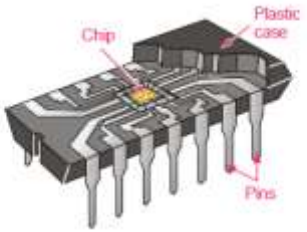
Yield



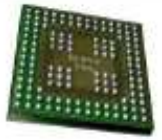
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

IC Packaging



- ICs are packaged in ceramic or plastic.

IC Packaging	Dual In-line Package (DIP)	Small Outline IC (SOIC)	Quad Flat Package (QFP)	Pin Grid Array (PGA)	Ball Grid Array (BGA)
Type	lead frame	lead frame	lead frame	area array	area array
Pins connected to	two sides	two sides	four sides	bottom	bottom
Lead count	< 64	< 80	$32 - 200$	$64 - 500$	$64 - 500$
Through hole Surface mount	Yes No	No Yes	No Yes	Yes Yes	Yes Yes
Cost	very low	very low	low	high	moderate
Electrical performance	very poor	poor	poor	optimized	better
Shrink version	Yes: SDIP	Yes: SSOIC	No	No	No
					

IC Technologies

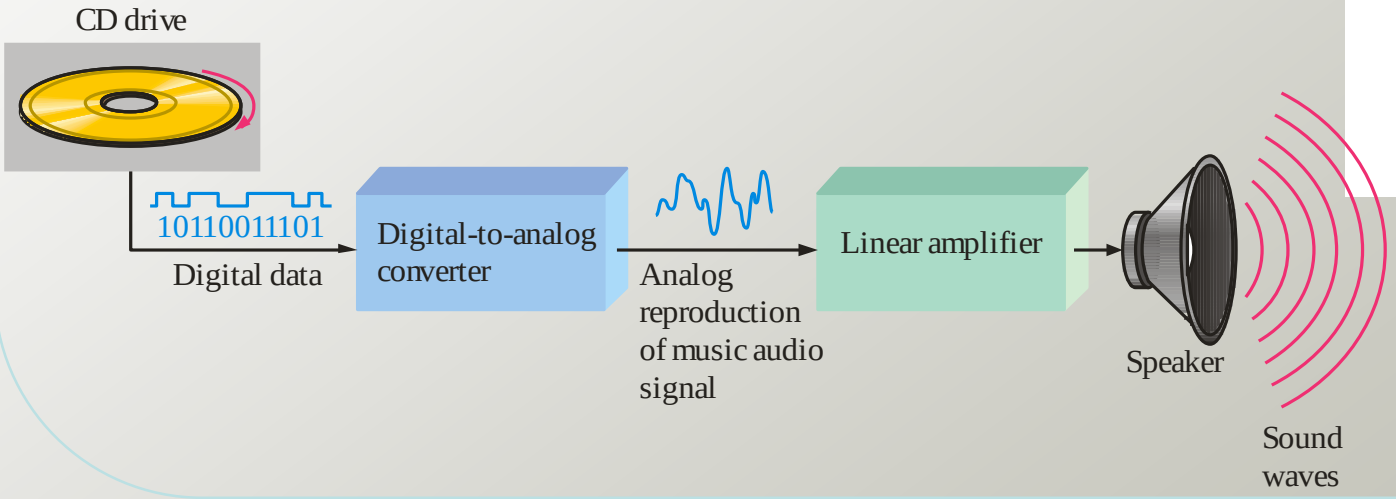
- ASIC (Application Specific Integrated Circuit)
  - ❑ Full Custom (Transistor Level)
  - ❑ Standard Cell (Gate Level – libraries)
  - ❑ Gate Array (Gate Level already created of the wafer)
- Filed Programmable Devices
  - ❑ Complex
    - **Complex Programmable Logic Devices (CPLD)**
    - **Field Programmable Gate Array (FPGA)**
  - ❑ Simple
    - **Programmable logic Devices (PLD)**
- Off-The-Shelf Components
  - ❑ MSI / SSI (Transistor Transistor Logic TTL - Series 7400), (Complementary Metal Oxide Semiconductor CMOS - Series 4000)

IC Complexity Scaling

- Small Scale Integration (SSI) [< 10 Gates]
  - Basic gates, flip flops.
- Medium Scale Integration (MSI) [<100 Gates]
  - Functions (decoders, encoders, counter, arithmetic units)
- Large Scale Integration (LSI) [<10,000 Gates]
  - Small systems (memories , small processors)
- Very Large Scale Integration (VLSI) [< 100,000 Gates]
  - Systems
- Ultra Large Scale Integration (ULSI)

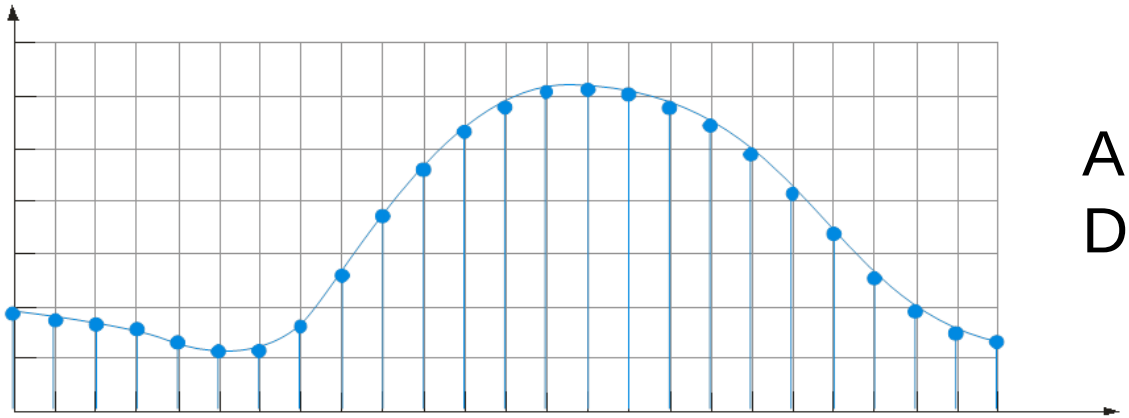
Digital System (Why)

- Easier to design.
- Flexibility and functionality.
  easier to store, transmit and manipulate information.
- Cheaper device.



Digital System (Why)
Analog vs. Digital

Most natural quantities (such as temperature, pressure, light intensity, …) are **analog** quantities that vary continuously.

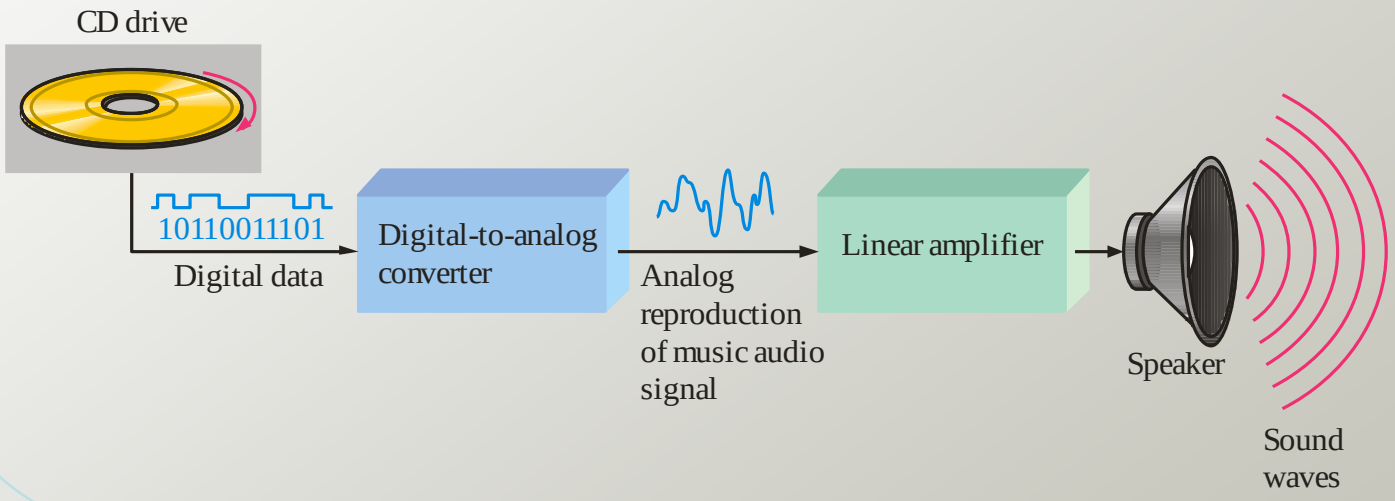


Analog = continuous
Digital = discrete

Digital systems can process, store, and transmit data more efficiently but can only assign discrete values to each point.

Digital System (Example)

- Wave Example



Digital Design Motivations

- Design for Functionality.
- Design for Integration.
- Design for Testability.
- Design for Performance.
- Design for Performance Monitoring.
- Design for Low Power.

Digital Design Metrics

- Cost.
- Area.
- Speed.
- Reliability.
- Power Dissipation.
- Time-to-Market.

Digital System Implementation Spectrum

Hardware
ASIC

Reconfigurable Architectures

- CPLD
- FPGA
- Customized Processors
- Coarse Grain

- Reconfigurable Array

Software

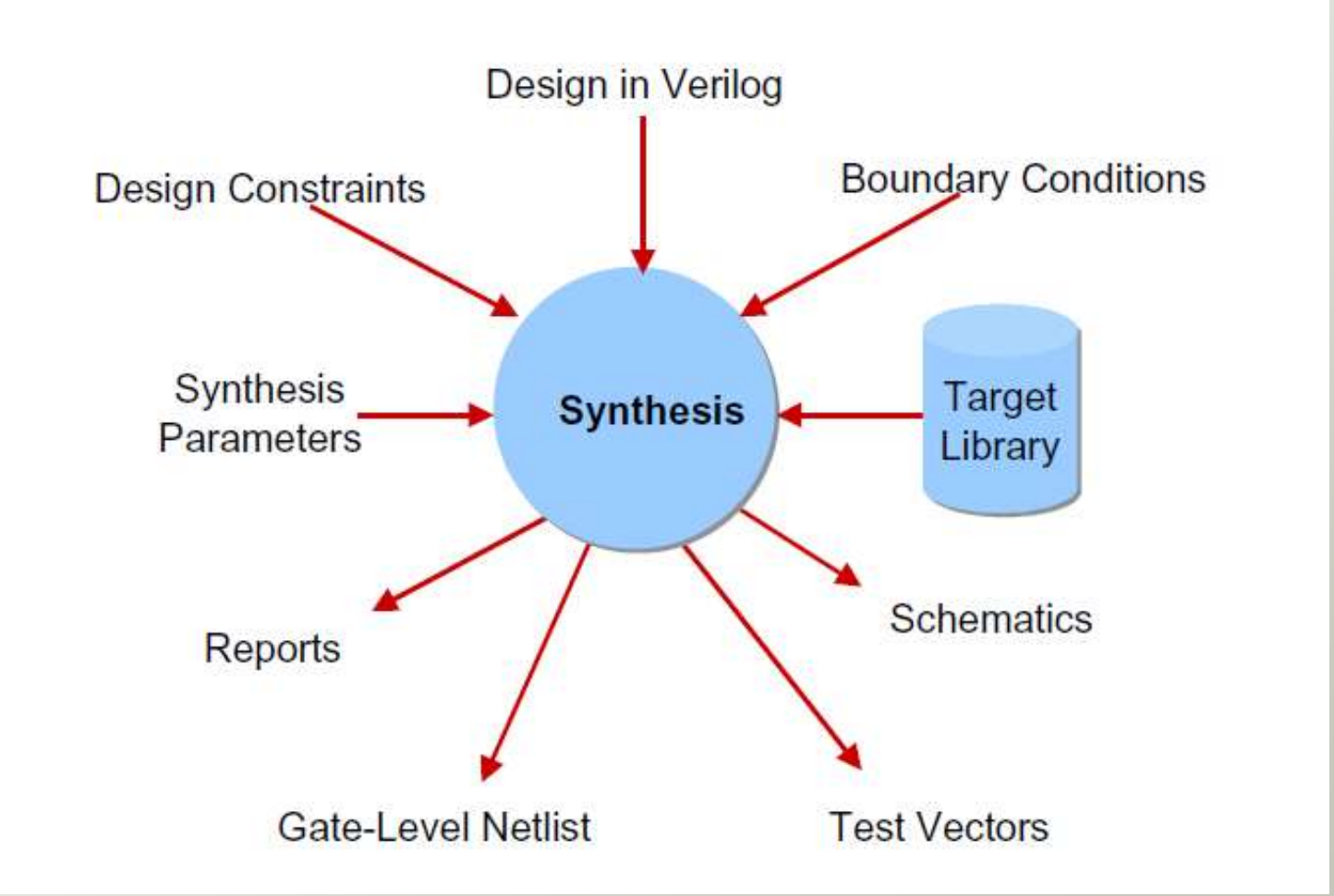
- µProcessor
- µController
- DSP

flexibility trade-off efficiency

Synthesis

- Synthesis is an automatic method of converting a higher level of abstraction (RTL) to a lower level of abstraction (gate level Netlists).
- Synthesis produces technology-specific implementation from technology-independent HDL description.
- Not all HDL can be used for synthesis. There are the HDL subset for synthesis and synthesis style description.
- Synthesis is very sensitive to how the HDL is written
  - Good design is still the responsibility of the designer.
  - Junk in - junk out

Synthesis Inputs and Outputs



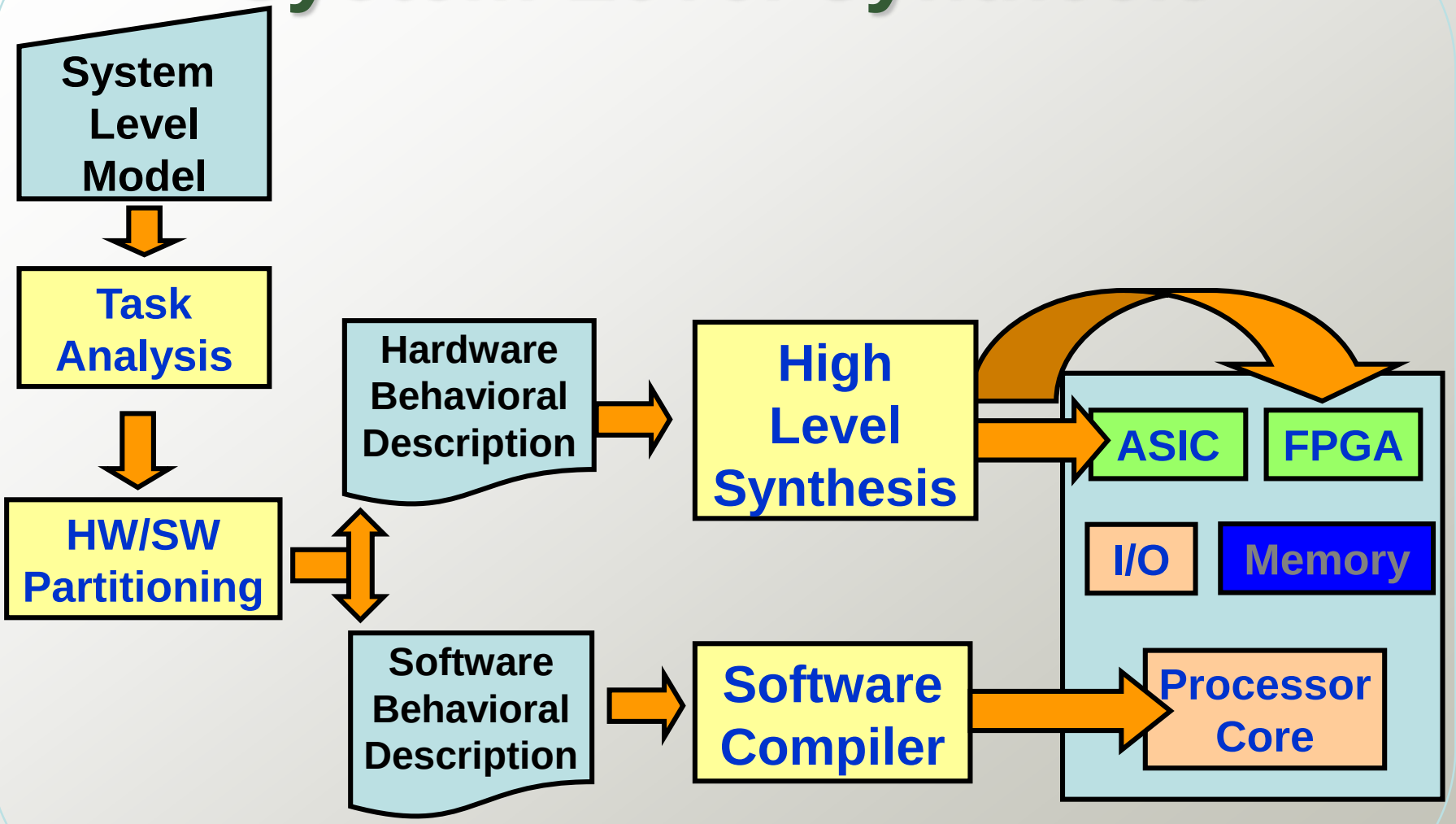
Digital Design Flow

- Design Flow (ASIC and FPGA)
  - Reading Specs from the customer.
  - Define the full definition of the problem.
  - Detailed Specs and architecture of the project.
  - Design the test structure specs and architecture
  - Behavioral design of the project (to test the idea)
  - Design entry
    - HDL , Schematic, State machine, Flow chart , Block diagram
  - HDL simulation (Function Simulation)
  - Logic Synthesis.
  - Post-Synthesis simulation. (FPGA)

Digital Design Flow

- Design Flow (ASIC Only)
  - Foundry and Technology
  - Mapping the design to the foundry library
  - ALG (Automatic Layout Generation)
  - Extraction of Parasitics.
  - DRC, ERC, LVS
  - Timing Simulation (Include Parasitics)
  - Redesign to meet the required specs.
  - Translate into GDSII format
  - Send for prototype fabrication
  - Wait for about 8 weeks
  - Design the PCB for the test
  - Test the Hardware
  - Mass production
  - Congratulation you will get a lot of money

System Level Synthesis



Electronics Shops

- https://store.fut-electronics.com/
- http://ram-e-shop.com/oscmax/catalog/